
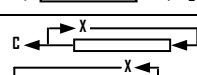
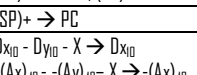


Opcode	Size	Operand	CCR	Effective Address s=source, d=destination, e=either, i=displacement										Operation	Description		
	BWL	s,d	XNZVC	Dn	An	(An)	(An)+	-(An)	(i,An)	(i,An,Rn)	abs.W	abs.L	(i,PC)	(i,PC,Rn)	#n		
ABCD	B	Dy,Dx -(Ay),-(Ax)	*U*U*	e	-	-	-	-	-	-	-	-	-	-	-	$D_{y10} + D_{x10} + X \rightarrow D_{x10}$ $-(Ay)_{10} + -(Ax)_{10} + X \rightarrow -(Ax)_{10}$	BCD destination + BCD source + eXtend Z cleared if result not 0 unchanged otherwise
ADD <sup>4</sup>	BWL	s,Dn Dn,d	*****	e	s <sup>4</sup>	s	s	s	s	s	s	s	s	s	s	$s + Dn \rightarrow Dn$ $Dn + d \rightarrow d$	Add binary (ADDI or ADDQ is used when source is #n. Prevent ADDQ with #n.L)
ADDA <sup>4</sup>	WL	s,An	-----	s	e	s	s	s	s	s	s	s	s	s	s	$s + An \rightarrow An$	Add address (.W sign-extended to .L)
ADDI <sup>4</sup>	BWL	#n,d	*****	d	-	d	d	d	d	d	d	d	-	-	s	$\#n + d \rightarrow d$	Add immediate to destination
ADDQ <sup>4</sup>	BWL	#n,d	*****	d	d	d	d	d	d	d	d	d	-	-	s	$\#n + d \rightarrow d$	Add quick immediate (#n range: 1 to 8)
ADDX	BWL	Dy,Dx -(Ay),-(Ax)	*****	e	-	-	-	-	-	-	-	-	-	-	-	$Dy + Dx + X \rightarrow Dx$ $-(Ay) + -(Ax) + X \rightarrow -(Ax)$	Add source and eXtend bit to destination
AND <sup>4</sup>	BWL	s,Dn Dn,d	---*00	e	-	s	s	s	s	s	s	s	s	s	s	$s \text{ AND } Dn \rightarrow Dn$ $Dn \text{ AND } d \rightarrow d$	Logical AND source to destination (ANDI is used when source is #n)
ANDI <sup>4</sup>	BWL	#n,d	---*00	d	-	d	d	d	d	d	d	d	-	-	s	$\#n \text{ AND } d \rightarrow d$	Logical AND immediate to destination
ANDI <sup>4</sup>	B	#n,CCR	====	-	-	-	-	-	-	-	-	-	-	-	s	$\#n \text{ AND } CCR \rightarrow CCR$	Logical AND immediate to CCR
ANDI <sup>4</sup>	W	#n,SR	====	-	-	-	-	-	-	-	-	-	-	-	s	$\#n \text{ AND } SR \rightarrow SR$	Logical AND immediate to SR (Privileged)
ASL	BWL	Dx,Dy	*****	e	-	-	-	-	-	-	-	-	-	-	-	$X \leftarrow X \ll 1$ $C \leftarrow X \gg 1$	Arithmetic shift Dy by Dx bits left/right
ASR	W	#n,Dy d		d	-	-	-	-	-	-	-	-	-	-	s	$X \leftarrow X \gg \#n$ $C \leftarrow X \ll 1$	Arithmetic shift Dy #n bits L/R (#n: 1 to 8) Arithmetic shift ds 1 bit left/right (.W only)
Bcc	BW <sup>4</sup>	address <sup>2</sup>	-----	-	-	-	-	-	-	-	-	-	-	-	-	if cc true then address $\rightarrow$ PC	Branch conditionally (cc table on back) (8 or 16-bit $\pm$ offset to address)
BCHG	B L	Dn,d #n,d	---*--	e'	-	d	d	d	d	d	d	d	-	-	-	$\text{NOT}(\text{bit number of } d) \rightarrow Z$ $\text{NOT}(\text{bit } n \text{ of } d) \rightarrow \text{bit } n \text{ of } d$	Set Z with state of specified bit in d then invert the bit in d
BCLR	B L	Dn,d #n,d	---*--	e'	-	d	d	d	d	d	d	d	-	-	-	$\text{NOT}(\text{bit number of } d) \rightarrow Z$ $0 \rightarrow \text{bit number of } d$	Set Z with state of specified bit in d then clear the bit in d
BFCHG	<sup>5</sup>	d{a:w}	---*00	d	-	d	-	-	-	d	d	d	-	-	-	$\text{NOT}$ bit field of d	Complement the bit field at destination
BFCLR	<sup>5</sup>	d{a:w}	---*00	d	-	d	-	-	-	d	d	d	-	-	-	$0 \rightarrow \text{bit field of } d$	Clear the bit field at destination
BFEXTS	<sup>5</sup>	s{a:w},Dn	---*00	d	-	s	-	-	-	s	s	s	s	s	s	bit field of s extend 32 $\rightarrow$ Dn	Dn = bit field of s sign extended to 32 bits
BFEXTU	<sup>5</sup>	s{a:w},Dn	---*00	d	-	s	-	-	-	s	s	s	s	s	s	bit field of s unsigned $\rightarrow$ Dn	Dn = bit field of s zero extended to 32 bits
BFFFO	<sup>5</sup>	s{a:w},Dn	---*00	d	-	s	-	-	-	s	s	s	s	s	s	bit number of 1 <sup>st</sup> I $\rightarrow$ Dn	Dn = bit position of 1 <sup>st</sup> I or offset + width
BFINs	<sup>5</sup>	Dn,s{a:w}	---*00	s	-	d	-	-	-	d	d	d	-	-	-	low bits Dn $\rightarrow$ bit field at d	Insert low bits of Dn to bit field at d
BFSET	<sup>5</sup>	d{a:w}	---*00	d	-	d	-	-	-	d	d	d	-	-	-	$1 \rightarrow \text{bit field of } d$	Set all bits in bit field of destination
BFTST	<sup>5</sup>	d{a:w}	---*00	d	-	d	-	-	-	d	d	d	-	-	-	set CCR with bit field of d	N = high bit of bit field, Z set if all bits 0
BRA	BW <sup>4</sup>	address <sup>2</sup>	-----	-	-	-	-	-	-	-	-	-	-	-	-	address $\rightarrow$ PC	Branch always (8 or 16-bit $\pm$ offset to addr)
BSET	B L	Dn,d #n,d	---*--	e'	-	d	d	d	d	d	d	d	-	-	-	$\text{NOT}(\text{bit } n \text{ of } d) \rightarrow Z$ $1 \rightarrow \text{bit } n \text{ of } d$	Set Z with state of specified bit in d then set the bit in d
BSR	BW <sup>4</sup>	address <sup>2</sup>	-----	-	-	-	-	-	-	-	-	-	-	-	-	PC $\rightarrow$ -(SP); address $\rightarrow$ PC	Branch to subroutine (8 or 16-bit $\pm$ offset)
BTST	B L	Dn,d #n,d	---*--	e'	-	d	d	d	d	d	d	d	-	-	-	$\text{NOT}(\text{bit } Dn \text{ of } d) \rightarrow Z$ $\text{NOT}(\text{bit } \#n \text{ of } d) \rightarrow Z$	Set Z with state of specified bit in d Leave the bit in d unchanged
CHK	W	s,Dn	-*UUU	e	-	s	s	s	s	s	s	s	s	s	s	if Dn < 0 or Dn > s then TRAP	Compare Dn with 0 and upper bound [s]
CLR	BWL	d	-0100	d	-	d	d	d	d	d	d	d	-	-	-	$0 \rightarrow d$	Clear destination to zero
CMP <sup>4</sup>	BWL	s,Dn	---***	e	s <sup>4</sup>	s	s	s	s	s	s	s	s	s	s	set CCR with Dn - s	Compare Dn to source
CMPA <sup>4</sup>	WL	s,An	---***	s	e	s	s	s	s	s	s	s	s	s	s	set CCR with An - s	Compare An to source
CMPI <sup>4</sup>	BWL	#n,d	---***	d	-	d	d	d	d	d	d	d	-	-	-	set CCR with d - #n	Compare destination to #n
CMPM <sup>4</sup>	BWL	(Ay)+,(Ax)+	---***	-	-	-	e	-	-	-	-	-	-	-	-	set CCR with (Ax) - (Ay)	Compare (Ax) to (Ay); Increment Ax and Ay
DBcc	W	Dn,address <sup>2</sup>	-----	-	-	-	-	-	-	-	-	-	-	-	-	if cc false then { Dn-1 $\rightarrow$ Dn if Dn <> -1 then addr $\rightarrow$ PC }	Test condition, decrement and branch (16-bit $\pm$ offset to address)
DIVS	W	s,Dn	---**0	e	-	s	s	s	s	s	s	s	s	s	s	$\pm 32\text{bit } Dn / \pm 16\text{bit } s \rightarrow \pm Dn$	Dn = [ 16-bit remainder, 16-bit quotient ]
DIVU	W	s,Dn	---**0	e	-	s	s	s	s	s	s	s	s	s	s	$32\text{bit } Dn / 16\text{bit } s \rightarrow Dn$	Dn = [ 16-bit remainder, 16-bit quotient ]
EOR <sup>4</sup>	BWL	Dn,d	---*00	e	-	d	d	d	d	d	d	d	-	-	s	$Dn \text{ XOR } d \rightarrow d$	Logical exclusive OR Dn to destination
EORI <sup>4</sup>	BWL	#n,d	---*00	d	-	d	d	d	d	d	d	d	-	-	s	$\#n \text{ XOR } d \rightarrow d$	Logical exclusive OR #n to destination
EORI <sup>4</sup>	B	#n,CCR	====	-	-	-	-	-	-	-	-	-	-	-	s	$\#n \text{ XOR } CCR \rightarrow CCR$	Logical exclusive OR #n to CCR
EORI <sup>4</sup>	W	#n,SR	====	-	-	-	-	-	-	-	-	-	-	-	s	$\#n \text{ XOR } SR \rightarrow SR$	Logical exclusive OR #n to SR (Privileged)
EXG	L	Rx,Ry	-----	e	e	-	-	-	-	-	-	-	-	-	-	register $\leftrightarrow$ register	Exchange registers (32-bit only)
EXT	WL	Dn	---*00	d	-	-	-	-	-	-	-	-	-	-	-	$Dn.B \rightarrow Dn.W \mid Dn.W \rightarrow Dn.L$	Sign extend (change .B to .W or .W to .L)
ILLEGAL			-----	-	-	-	-	-	-	-	-	-	-	-	-	PC $\rightarrow$ -(SSP); SR $\rightarrow$ -(SSP)	Generate Illegal Instruction exception
JMP		d	-----	-	-	d	-	-	-	d	d	d	d	d	-	$\uparrow d \rightarrow PC$	Jump to effective address of destination
JSR		d	-----	-	-	d	-	-	-	d	d	d	d	d	-	PC $\rightarrow$ -(SP); $\uparrow d \rightarrow PC$	push PC, jump to subroutine at address d
LEA	L	s,An	-----	-	e	s	-	-	-	s	s	s	s	s	-	$\uparrow s \rightarrow An$	Load effective address of s to An
LINK		An,#n	-----	-	-	-	-	-	-	-	-	-	-	-	-	An $\rightarrow$ -(SP); SP $\rightarrow$ An; SP + #n $\rightarrow$ SP	Create local workspace on stack (negative n to allocate space)
LSL	BWL	Dx,Dy #n,Dy	***0*	e	-	-	-	-	-	-	-	-	-	-	-	$X \leftarrow X \ll 1$ $C \leftarrow X \gg 1$	Logical shift Dy, Dx bits left/right
LSR	W	d		d	-	-	-	-	-	-	-	-	-	-	s	$X \leftarrow X \gg \#n$ $C \leftarrow X \ll 1$	Logical shift Dy, #n bits L/R (#n: 1 to 8) Logical shift d 1 bit left/right (.W only)
MOVE <sup>4</sup>	BWL	s,d	---*00	e	s <sup>4</sup>	e	e	e	e	e	e	e	s	s	s	$s \rightarrow d$	Move data from source to destination
MOVE	W	s,CCR	====	s	-	s	s	s	s	s	s	s	s	s	s	$s \rightarrow CCR$	Move source to Condition Code Register
MOVE	W	s,SR	====	s	-	s	s	s	s	s	s	s	s	s	s	$s \rightarrow SR$	Move source to Status Register (Privileged)
MOVE	W	SR,d	-----	d	-	d	d	d	d	d	d	d	-	-	-	$SR \rightarrow d$	Move Status Register to destination
	BWL	s,d	XNZVC	Dn	An	(An)	(An)+	-(An)	(i,An)	(i,An,Rn)	abs.W	abs.L	(i,PC)	(i,PC,Rn)	#n		

Opcode	Size	Operand	CCR	Effective Address s=source, d=destination, e=either, i=displacement											Operation	Description	
	BWL	s,d	XNZVC	Dn	An	(An)	(An)+	-(An)	(i,An)	(i,An,Rn)	abs.W	abs.L	(i,PC)	(i,PC,Rn)	#n		
MOVE	L	USP,An An,USP	-----	-	d	-	-	-	-	-	-	-	-	-	-	USP → An An → USP	Move User Stack Pointer to An (Privileged) Move An to User Stack Pointer (Privileged)
MOVEA <sup>4</sup>	WL	s,An	-----	s	e	s	s	s	s	s	s	s	s	s	s	s → An	Move source to An (MOVE s,An use MOVEA)
MOVEM <sup>4</sup>	WL	Rn-Rn,d s,Rn-Rn	-----	-	-	d	-	d	d	d	d	d	-	-	-	Registers → d s → Registers	Move specified registers to/from memory (.W source is sign-extended to .L for Rn)
MOVEP	WL	Dn,(i,An) (i,An),Dn	-----	s	-	-	-	-	d	-	-	-	-	-	-	Dn → (i,An)...(i+2,An)...(i+4,An) (i,An) → Dn...(i+2,An)...(i+4,An)	Move Dn to/from alternate memory bytes (Access only even or odd addresses)
MOVEQ <sup>4</sup>	L	#n,Dn	-**000	d	-	-	-	-	-	-	-	-	-	-	-	#n → Dn	Move sign extended 8-bit #n to Dn
MULS	W	s,Dn	-**000	e	-	s	s	s	s	s	s	s	s	s	s	±16bit s * ±16bit Dn → ±Dn	Multiply signed 16-bit; result: signed 32-bit
MULU	W	s,Dn	-**000	e	-	s	s	s	s	s	s	s	s	s	s	16bit s * 16bit Dn → Dn	Multiply unsigned 16-bit; result: unsigned 32-bit
NBCD	B	d	*U*U*	d	-	d	d	d	d	d	d	d	-	-	-	0 - d <sub>10</sub> - X → d	Negate BCD with eXtend, BCD result
NEG	BWL	d	*****	d	-	d	d	d	d	d	d	d	-	-	-	0 - d → d	Negate destination (2's complement)
NEGX	BWL	d	*****	d	-	d	d	d	d	d	d	d	-	-	-	0 - d - X → d	Negate destination with eXtend
NOP			-----	-	-	-	-	-	-	-	-	-	-	-	-	None	No operation occurs
NOT	BWL	d	-**000	d	-	d	d	d	d	d	d	d	-	-	-	NOT(d) → d	Logical NOT destination (1's complement)
OR <sup>4</sup>	BWL	s,Dn Dn,d	-**000	e	-	s	s	s	s	s	s	s	s	s	s <sup>4</sup>	s OR Dn → Dn Dn OR d → d	Logical OR (ORI is used when source is #n)
ORI <sup>4</sup>	BWL	#n,d	-**000	d	-	d	d	d	d	d	d	d	-	-	s	#n OR d → d	Logical OR #n to destination
ORI <sup>4</sup>	B	#n,CCR	=====	-	-	-	-	-	-	-	-	-	-	-	s	#n OR CCR → CCR	Logical OR #n to CCR
ORI <sup>4</sup>	W	#n,SR	=====	-	-	-	-	-	-	-	-	-	-	-	s	#n OR SR → SR	Logical OR #n to SR (Privileged)
PEA	L	s	-----	-	-	s	-	-	s	s	s	s	s	s	s	↑s → -(SP)	Push effective address of s onto stack
RESET			-----	-	-	-	-	-	-	-	-	-	-	-	-	Assert RESET Line	Issue a hardware RESET (Privileged)
ROL	BWL	Dx,Dy	-**0*	e	-	-	-	-	-	-	-	-	-	-	-		Rotate Dy, Dx bits left/right (without X)
ROR	W	#n,Dy d	-	d	-	-	-	-	-	-	-	-	-	-	-		Rotate Dy, #n bits left/right (#n: 1 to 8) Rotate d l-bit left/right (.W only)
ROXL	BWL	Dx,Dy	***0*	e	-	-	-	-	-	-	-	-	-	-	-		Rotate Dy, Dx bits L/R, X used then updated
ROXR	W	#n,Dy d	-	d	-	d	d	d	d	d	d	d	-	-	-		Rotate Dy, #n bits left/right (#n: 1 to 8) Rotate destination l-bit left/right (.W only)
RTE			=====	-	-	-	-	-	-	-	-	-	-	-	-	(SP)+ → SR; (SP)+ → PC	Return from exception (Privileged)
RTR			=====	-	-	-	-	-	-	-	-	-	-	-	-	(SP)+ → CCR; (SP)+ → PC	Return from subroutine and restore CCR
RTS			-----	-	-	-	-	-	-	-	-	-	-	-	-	(SP)+ → PC	Return from subroutine
SBCD	B	Dy,Dx -(Ay),-(Ax)	*U*U*	e	-	-	-	-	-	-	-	-	-	-	-	Dx <sub>10</sub> - Dy <sub>10</sub> - X → Dx <sub>10</sub> -(Ax) <sub>10</sub> - (Ay) <sub>10</sub> - X → -(Ax) <sub>10</sub>	BCD destination - BCD source - eXtend Z cleared if result not 0 unchanged otherwise
SCC	B	d	-----	d	-	d	d	d	d	d	d	d	-	-	-	If cc is true then 1's → d else 0's → d	If cc true then d.B = 11111111 else d.B = 00000000
STOP		#n	=====	-	-	-	-	-	-	-	-	-	-	-	s	#n → SR; STOP	Move #n to SR, stop processor (Privileged)
SUB <sup>4</sup>	BWL	s,Dn Dn,d	*****	e	s	s	s	s	s	s	s	s	s	s	s <sup>4</sup>	Dn - s → Dn d - Dn → d	Subtract binary (SUBI or SUBQ used when source is #n. Prevent SUBQ with #n.L)
SUBA <sup>4</sup>	WL	s,An	-----	s	e	s	s	s	s	s	s	s	s	s	s	An - s → An	Subtract address (.W sign-extended to .L)
SUBI <sup>4</sup>	BWL	#n,d	*****	d	-	d	d	d	d	d	d	d	-	-	s	d - #n → d	Subtract immediate from destination
SUBQ <sup>4</sup>	BWL	#n,d	*****	d	d	d	d	d	d	d	d	d	-	-	s	d - #n → d	Subtract quick immediate (#n range: 1 to 8)
SUBX	BWL	Dy,Dx -(Ay),-(Ax)	*****	e	-	-	-	-	-	-	-	-	-	-	-	Dx - Dy - X → Dx -(Ax) - (Ay) - X → -(Ax)	Subtract source and eXtend bit from destination
SWAP	W	Dn	-**000	d	-	-	-	-	-	-	-	-	-	-	-	bits[31:16] ↔ bits[15:0]	Exchange the 16-bit halves of Dn
TAS	B	d	-**000	d	-	d	d	d	d	d	d	d	-	-	-	test d → CCR; 1 → bit7 of d	N and Z set to reflect d, bit7 of d set to 1
TRAP		#n	-----	-	-	-	-	-	-	-	-	-	-	-	s	PC → -(SSP); SR → -(SSP); (vector table entry) → PC	Push PC and SR, PC set by vector table #n (#n range: 0 to 15)
TRAPV			-----	-	-	-	-	-	-	-	-	-	-	-	-	If V then TRAP #7	If overflow, execute an Overflow TRAP
TST	BWL	d	-**000	d	-	d	d	d	d	d	d	d	-	-	-	test d → CCR	N and Z set to reflect destination
UNLK		An	-----	-	d	-	-	-	-	-	-	-	-	-	-	An → SP; (SP)+ → An	Remove local workspace from stack

Condition Tests (+ OR, !NOT, ⊕ XOR; * Unsigned, # Alternate cc)					
cc	Condition	Test	cc	Condition	Test
T	true	I	VC	overflow clear	!V
F	false	O	VS	overflow set	V
HI <sup>#</sup>	higher than	!(C + Z)	PL	plus	!N
LS <sup>#</sup>	lower or same	C + Z	MI	minus	N
HS <sup>#</sup> , CC <sup>#</sup>	higher or same	!C	GE	greater or equal	!(N ⊕ V)
LO <sup>#</sup> , CS <sup>#</sup>	lower than	C	LT	less than	(N ⊕ V)
NE	not equal	!Z	GT	greater than	!(N ⊕ V) + Z
EQ	equal	Z	LE	less or equal	(N ⊕ V) + Z

**An** Address register (16/32-bit, n=0-7)  
**Dn** Data register (8/16/32-bit, n=0-7)  
**Rn** any data or address register  
**BCD** Binary Coded Decimal  
**PC** Program Counter (24-bit)  
**#n** Immediate data  
**SP** Active Stack Pointer (same as A7)  
<sup>1</sup> Long only; all others are byte only  
<sup>3</sup> Branch sizes: **B** or **S** -128 to +127 bytes, **W** or **L** -32768 to +32767 bytes  
<sup>4</sup> Assembler automatically uses A, I, Q or M form if possible. Use #n.L to prevent Quick optimization  
<sup>5</sup> Bit field determines size. Not supported by 68000. EASy68K hybrid form of 68020 instruction

**SR** Status Register (16-bit)  
**CCR** Condition Code Register (lower 8-bits of SR)  
**N** negative, **Z** zero, **V** overflow, **C** carry, **X** extend  
 \* set by operation's result, ≡ set directly  
 - not affected, **O** cleared, **I** set, **U** undefined

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**Commonly Used Simulator Input/Output Tasks** TRAP #15 is used to run simulator tasks. Place the task number in register D0. See Help for a complete description of available tasks. (cstring is null terminated)

<b>0</b>	Display n characters of string at (A1), n=D1.W (stops on NULL or max 255) with CR,LF	<b>1</b>	Display n characters of string at (A1), n=D1.W (stops on NULL or max 255) without CR,LF	<b>2</b>	Read characters from keyboard. Store at (A1). Null terminated. D1.W = length (max 80)	<b>3</b>	Display D1.L as signed decimal number
<b>4</b>	Read number from keyboard into D1.L	<b>5</b>	Read single character from keyboard in D1.B	<b>6</b>	Display D1.B as ASCII character	<b>7</b>	Set D1.B to 1 if keyboard input pending else set to 0
<b>8</b>	time in 1/100 second since midnight → D1.L	<b>9</b>	Terminate the program. (Halts the simulator)	<b>10</b>	Print cstring at (A1) on default printer.	<b>11</b>	Position cursor at row,col D1.W=ccrr; \$FF00 clears
<b>13</b>	Display cstring at (A1) with CR,LF	<b>14</b>	Display cstring at (A1) without CR,LF	<b>15</b>	Display unsigned number in D1.L in D2.B base	<b>17</b>	Display cstring at (A1), then display number in D1.L
<b>18</b>	Display cstring at (A1), read number into D1.L	<b>19</b>	Return state of keys or scan code. See help	<b>20</b>	Display ± number in D1.L, field D2.B columns wide	<b>21</b>	Set font properties. See help for details